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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,609	TANIGAWA ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *May 19, 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received June 28, 2006 for application number 10/637,609 originally filed August 11, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: an unmarked replacement Specification; a marked-up, amended Specification (which includes a marked-up, amended Abstract on page 47); an unmarked, replacement Abstract; and, amended claims 1-34.

Information Disclosure Statement

The Information Disclosure Statement (IDS) submitted on May 19, 2006 was placed of record in file. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement is being considered by the Examiner.

Abstract

The replacement Abstract received June 28, 2006 has been accepted.

Specification

The amendment filed June 28, 2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the example added to the Specification, "(i.e.,

using at least a portion of the memory 107 a plurality of times)" which is new matter to both the Specification and all the independent Claims (Specification, page 18, lines 17-23).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 and 11-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This new matter, also newly added to the Specification (as objected to hereinabove), is found on: claim 1, lines 10-11 and 14-15; claim 2, lines 11-12 and 16-17; claim 3, lines 11-12 and 16-17; claim 4, lines 12-13 and 18-19; claim 5, lines 14-15 and 22-23; claim 11, lines 5-6 and 12-13; claim 12, lines 17-21; claim 13, lines 6-7 and 11-12; and, claim 14, lines 18-19 and 22-23.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okayama et al. (U.S. Patent No. 5,045,939) (hereinafter referred to as Okayama) in view of Takabatake et al. (U.S. Patent No. 6,320,909 B1) (hereinafter referred to as Takabatake) and Stam et al. (U.S. Patent No. 6,631,316 B2) (hereinafter referred to as Stam).

As to claims 1-5, which are all rejected for containing similar data, Okayama discloses a clock conversion apparatus for converting data synchronized with a first clock (22) into data synchronized with a second clock (23), the clocking conversion apparatus comprising: a memory (25) for storage being able to execute a writing operation and a reading operation independently from each other using a clock for writing (22) and a clock for reading (23), respectively (Okayama discloses writing and reading operations handled independently from each other using their own clocks and counters to carry out addressing of and reading of said data; column 3, lines 30-35 and column 3, lines 54-57); a first counter (27) for starting count of the first clock on receipt of a writing start reference signal (receiving the first clock signal when the horizontal sync signal is delivered) indicating a reference timing of starting data writing into the memory and generating write addresses (column 3, lines 17-22 and column 3, lines 30-35) of the memory

so that the write addresses repeat increase or decrease (counts up in response to the first clock signal) within a predetermined range of addresses of the memory (Okayama discloses extracting data from wide screen picture data stored in memory 25 therefore knowing the size of the image captured before storage; column 3, lines 10-16), thereby enabling writing of the data corresponding to the predetermined period into the memory over plural times (column 3, lines 36-53); a second counter (28) for starting count of the second clock from a reading start reference signal (receiving the first clock signal when the horizontal sync signal is delivered) indicating a reference timing of starting data reading from the memory and generating read addresses (column 3, lines 17-22; column 3, lines 36-39; column 3, lines 54-57) of the memory so that the read addresses repeat increase or decrease (counts up from the start address) within a predetermined range of addresses of the memory (Okayama discloses being aware of the number of data to be extracted for normal screen size of the starting of the reading process; column 3, line 57 thru column 4, line 3), thereby enabling reading of the data corresponding to the predetermined period, which have been written in the memory, over plural times (column 3, lines 36-53).

Okayama does not disclose a delay adjustment circuit operable to adjust a delay time, which delays the writing start reference signal to generate the reading start reference signal.

Takabatake teaches a picture decoding and display unit that contains a delay circuit (60) that is coupled to control unit (14) that enables address generator (54) which generates read addresses from memory banks (32, 34, 36) that is delayed from starting decoding of the data upon reception of a synchronization signal (column 16, lines 22-45 and column 17, line 60 thru column 1, line 16). Takabatake also has the additional benefit of reducing the storage capacity of

a memory unit that can also decode and display picture data while efficiently utilize a memory device (column 6, lines 61-67).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama and Takabatake before him at the time the invention was made, to modify address writing and reading scheme disclosed by Okayama to use the delay circuit as taught by Takabatake wherein the reading address creation process is delayed upon the reception of a synchronization signal. One of ordinary skill in the art would be motivated to make use of the delay circuit in view of the teachings of Takabatake, as doing so would give the added benefit of reducing the storage capacity of a memory unit that can also decode and display picture data while efficiently utilize a memory device (as taught above by Takabatake).

Though they both contain memory, neither Okayama nor Takabatake teach a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period of memory wherein writing and reading into and out of memory is done using at least a portion of the addresses of the memory a plurality of times. Also, Okayama and Takabatake do not teach the last address created for every predetermined period is carried out within a range of addresses narrower than the predetermined range of addresses.

Stam teaches an image processing system for storing image data with less available memory than is needed to store all pixel data (column 2, lines 18-23). Stam continues to teach that the amount of memory required is reduced by acquiring and analyzing only a portion of the image (using at least a portion of the addresses of the memory) wherein processing is carried out using nesting loops repetitively (plurality of times) until the process is done (see figure 4a). Stam also teaches discarding some of the image data collected to accommodate the reduced memory

available thereby narrowing the address range (column 8, lines 44-61). Stam has the additional benefit of lower the cost of image processing (column 1, line 66 thru column 2, line 2).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama, Takabatake and Stam before him at the time the invention was made, to modify memory disclosed by Okayama and Takabatake to use memory as taught by Stam wherein there is less available memory than is needed to store all data. One of ordinary skill in the art would be motivated to make use of the memory in view of the teachings of Stam, as doing so would give the added benefit of lowering the cost of image processing (as taught by Stam above).

As to claims 6 and 15-18, Okuyama in combination with Takabatake and Stam taught the clock conversion apparatus of claims 1-5, as shown above. Okuyama further teaches the clock conversion apparatus wherein the data corresponding to the predetermined period are written in the memory (25) using write addresses (WA produced by the clock 22 and the counter 27) sampled at the first clock (22) within the predetermined period (column 3, lines 17-22 and column 3, lines 30-53); and, the data are read from the memory (25) using read addresses (RA produced by clock 23 and counter 28) sampled at the second clock (column 3, lines 17-22 and column 3, lines 30-57).

Stam further teaches discarding some picture data if memory size is inadequate to accommodate storage (column 8, lines 44-61). Also, Sham teaches saving picture data with the knowledge of minimum and maximum range data available to better and the ability to adjust row and column numbers as needed to accommodate image data (column 9, line 32 thru column 10, line 8).

As to claims 7 and 19-22, Okuyama in combination with Takabatake and Stam taught the clock conversion apparatus of claims 1-5, as shown above. Okuyama further teaches the clock conversion apparatus wherein the data corresponding to the predetermined period are written in the memory (25) using write addresses (WA produced by the clock 22 and the counter 27) sampled at the first clock (22) within the predetermined period (column 3, lines 17-22 and column 3, lines 30-53); and, the data are read from the memory (25) using read addresses (RA produced by clock 23 and counter 28) of the write addresses (with use of the start address SA generator 29; column 3, lines 17-22 and column 3, lines 30-57).

Stam further teaches discarding some picture data if memory size is inadequate to accommodate storage (column 8, lines 44-61).

Takabatake further teaches the read addresses have a maximum value equal to the maximum value of the write addresses (column 7, lines 11-23).

As to claims 8 and 23-26, Okuyama in combination with Takabatake and Stam taught the clock conversion apparatus of claims 1-5, as shown above. Okuyama further teaches the clock conversion apparatus wherein the predetermined period is one horizontal sync period (column 3, lines 17-35).

Claims 9 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okayama et al. (U.S. Patent No. 5,045,939), Takabatake et al. (U.S. Patent No. 6,320,909 B1) and Stam et al. (U.S. Patent No. 6,631,316 B2) as applied to claims 1-5 above, and further in view of Maze (U.S. Patent No. 4,573,080) (hereinafter referred to as Maze).

As to claims 9 and 27-30, neither Okayama, Takabatake nor Stam teach a write maximum value limiter for comparing the write address outputted from the write address counter

with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Maze teaches a television receiver with an adaptive memory addressing comprising a memory (24) for storing image data and write address generating circuitry. The write address generating circuitry comprises address comparator circuit (208) for comparing the write address outputted from a write address counter (202) with a settable write maximum value (highest address level), and resetting the write address counter (202) when the write address becomes equal to the write maximum value (column 6, lines 3-34). Maze has the additional feature of supporting a progressively scanned image data (column 1, line 55 thru column 2, line 3)

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama, Takabatake, Stam and Maze before him at the time the invention was made, to modify write counter circuit disclosed by Okayama to use the write address generation scheme as taught by Maze wherein writing of data is halted once a maximum write address limit is obtained. One of ordinary skill in the art would be motivated to make use of the write address generation in view of the teachings of Maze, as doing so would give the added benefit of supporting a progressively scanned image data (as taught by Maze above).

Claims 10 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okayama et al. (U.S. Patent No. 5,045,939), Takabatake et al. (U.S. Patent No. 6,320,909 B1) and Stam et al. (U.S. Patent No. 6,631,316 B2) as applied to claims 1-5 above, and further in view of Eglit (U.S. Patent No. 6,054,980) (hereinafter referred to as Eglit).

As to claims 10 and 31-34, neither Okayama, Takabatake nor Stam teach a read maximum value limiter for comparing the read address outputted from the read address counter

with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

Eglit teaches a display unit comprising a memory (560) for storing image data and addressing control circuitry (390). The addressing control circuitry (390) comprises read address comparator circuit (450) for comparing the last read address outputted from a read address counter (440) with a highest read address level, and resetting the read address counter (440) when the read address becomes equal to the read maximum value (column 9, lines 8-15). Eglit has the additional feature of frame rate compression without requiring excessive memory (column 2, lines 38-44).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama, Takabatake, Stam and Eglit before him at the time the invention was made, to modify read counter circuit disclosed by Okayama et al to use the read address generation scheme as taught by Eglit wherein reading of data is halted once a maximum read address limit is obtained. One of ordinary skill in the art would be motivated to make use of the read address generation in view of the teachings of Eglit, as doing so would give the added benefit of frame rate compression without requiring excessive memory (as taught by Eglit above).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okayama (as cited above) and Stam (as cited above).

As to claim 11, Okayama discloses a clock conversion method for converting data synchronized with a first clock (22) into data synchronized with a second clock (23), said method comprising: generating write addresses on the basis of the first clock (22) so that data corresponding to a predetermined period (as determined by write rate of data 17.6 MHz; column

3, lines 40-53) are written over plural times into a memory (25), and is able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading (Okayama discloses writing and reading operations handled independently from each other using their own clocks and counters to carry out addressing of and reading of said data; column 3, lines 30-57), respectively; and, generating read addresses on the basis of the second clock (23) so that the data corresponding to the predetermined period (as determined by read rate of data 14.3 MHz; column 3, lines 40-53) are read from the memory (25) over plural times (column 3, lines 30-57).

Okayama does not disclose a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period wherein writing and reading into and out of memory is done using at least a portion of the addresses of the memory a plurality of times.

Stam teaches an image processing system for storing image data with less available memory than is needed to store all pixel data (column 2, lines 18-23). Stam continues to teach that the amount of memory required is reduced by acquiring and analyzing only a portion of the image (using at least a portion of the addresses of the memory) wherein processing is carried out using nesting loops repetitively (plurality of times) until the process is done (see figure 4a). Stam also teaches discarding some of the image data collected to accommodate the reduced memory available thereby narrowing the address range (column 8, lines 44-61). Stam has the additional benefit of lower the cost of image processing (column 1, line 66 thru column 2, line 2).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama and Stam before him at the time the invention was made, to modify memory disclosed

by Okayama to use memory as taught by Stam wherein there is less available memory than is needed to store all data. One of ordinary skill in the art would be motivated to make use of the memory in view of the teachings of Stam, as doing so would give the added benefit of lowering the cost of image processing (as taught by Stam above).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (U.S. Patent No. 6,791,623 B1) (hereinafter referred to as Matsuda) and Stam (as cited above).

As to claim 12, Masuda discloses a video display apparatus (image display system) comprising: a first video processing unit (2) for subjecting a digital video signal (NTSC data) to first video processing (2) on the basis of a first clock (data coming in from A/D converter 42 are controlled in sync with the horizontal synchronization signal and write clock generator circuit [first clock] 416 via write control circuit; column 14, line 33 thru column 15, line 11 and column 18, line 58 thru column 19, line 20); a clock conversion unit (frequency resolution conversion unit 4) for converting the digital video signal which is outputted from the first video processing unit (2) and synchronized with the first clock (416) into a digital video signal synchronized with a second clock (read clock generator circuit 417; column 14, line 33 thru column 15, line 11 and column 18, line 58 thru column 19, line 20); a second video processing unit (5) for subjecting the digital video signal outputted from the clock conversion unit (4) to second video processing (5) on the basis of the second clock (read clock generator circuit 417 via read control circuit 410; column 14, lines 42-56 and column 18, line 58 thru column 19, line 20); a display device (7) for displaying the digital video signal outputted from the second video processing unit (column 14, lines 42-56); and, said clock conversion unit comprising: a memory (412 and 418) able to execute a writing operation and a reading operation independently from each other using a clock

for writing and a clock (416) for reading (417), (column 18, line 65 thru column 19, line 8) respectively; and, a memory controller (49 and 410) for controlling the memory so that the digital video signal outputted from the first video processing unit are written into the memory over plural times for every horizontal line, and the data corresponding to each horizontal line, which are written in the memory, can be read over plural times (Masuda discloses writing and reading operations wherein both are carried out repetitively until all subsequent lines of video data are read; column 16, lines 1-53).

Masuda does not disclose memory having a capacity less than one horizontal line of the digital video signal outputted from the first video processing unit wherein writing and reading into and out of memory is done using at least a portion of the addresses of the memory a plurality of times.

Stam teaches an image processing system for storing image data with less available memory than is needed to store all pixel data (column 2, lines 18-23). Stam continues to teach that the amount of memory required is reduced by acquiring and analyzing only a portion of the image (using at least a portion of the addresses of the memory) wherein processing is carried out using nesting loops repetitively (plurality of times) until the process is done (see figure 4a). Stam also teaches discarding some of the image data collected to accommodate the reduced memory available thereby narrowing the address range (column 8, lines 44-61). Stam has the additional benefit of lower the cost of image processing (column 1, line 66 thru column 2, line 2).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama and Stam before him at the time the invention was made, to modify memory disclosed by Okayama to use memory as taught by Stam wherein there is less available memory than is

needed to store all data. One of ordinary skill in the art would be motivated to make use of the memory in view of the teachings of Stam, as doing so would give the added benefit of lowering the cost of image processing (as taught by Stam above).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda (as cited above) and Stam (as cited above) as applied to claim 12 above, and further in view of Okayama (as cited above).

As to claim 13, neither Masuda nor Stam teaches a memory controller comprising a first counter circuit for starting count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the one horizontal line of data can be written into the memory over plural times; and a second counter circuit for starting count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the one horizontal line of data which are written in the memory can be read over plural times.

Okayama teaches a television screen converter comprising memory addressing circuitry comprising a memory (25), a write clock generator (22), a read clock generator (23), a write address counter (27), a read start address generator (29) and a read address counter (28). The write counter circuit (27) starts counting on receipt of a writing start reference signal (horizontal sync signal from sync separator 21) indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the one horizontal line of data can be written into the memory over plural times (column 3, lines 1-60). The read counter circuit (28) for start counting from a reading start reference signal (from read start address generator 29)

indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the one horizontal line of data which are written in the memory can be read over plural times (column 3, lines 1-60). Okayama has the additional benefit of automatically extracting and converting data from a wide screen version to a normal screen version (column 2, lines 11-17).

It would have been obvious to one of ordinary skill of the art, having the teachings of Masuda, Stam and Okayama before him at the time the invention was made, to modify memory controllers disclosed by Masuda to use memory addressing circuitry as taught by Okayama. One of ordinary skill in the art would be motivated to make use of the memory addressing circuitry in view of the teachings of Okayama, as doing so would give the added benefit of automatically extracting and converting data from a wide screen version to a normal screen version (as taught by Okayama above).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda (as cited above) in view of Stam (as cited above), Okayama (as cited above) and Worrell et al. (U.S. Patent No. 6,633,344 B1) (hereinafter referred to as Worrell).

As to claim 14, Masuda discloses a memory address setting method for a video display apparatus comprising: a first video processing unit (2) for subjecting a digital video signal (NTSC data) to first video processing on the basis of a first clock (data coming in from A/D converter 42 are controlled in sync with the horizontal synchronization signal and write clock generator circuit [first clock] 416 via write control circuit; column 14, line 33 thru column 15, line 11 and column 18, line 58 thru column 19, line 20); a clock conversion unit (frequency resolution conversion unit 4) for converting the digital video signal which is outputted from the

first video processing unit (2) and synchronized with the first clock (416) into a digital video signal synchronized with a second clock (read clock generator circuit 417; column 14, line 33 thru column 15, line 11 and column 18, line 58 thru column 19, line 20); a second video processing unit (5) for subjecting the digital video signal outputted from the clock conversion unit (4) to second video processing (5) on the basis of the second clock (read clock generator circuit 417 via read control circuit 410; column 14, lines 42-56 and column 18, line 58 thru column 19, line 20); a display device (7) for displaying the digital video signal outputted from the second video processing unit (column 14, lines 42-56); and, said clock conversion unit (frequency resolution conversion unit 4) comprising: a memory (412 and 418) able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock (416) for reading (417), (column 18, line 65 thru column 19, line 8).

Masuda does not disclose memory having a capacity less than one horizontal line of the digital video signal outputted from the first video processing unit wherein writing and reading into and out of memory is done using at least a portion of the addresses of the memory a plurality of times.

Stam teaches an image processing system for storing image data with less available memory than is needed to store all pixel data (column 2, lines 18-23). Stam continues to teach that the amount of memory required is reduced by acquiring and analyzing only a portion of the image (using at least a portion of the addresses of the memory) wherein processing is carried out using nesting loops repetitively (plurality of times) until the process is done (see figure 4a). Stam also teaches discarding some of the image data collected to accommodate the reduced memory

available thereby narrowing the address range (column 8, lines 44-61). Stam has the additional benefit of lower the cost of image processing (column 1, line 66 thru column 2, line 2).

It would have been obvious to one of ordinary skill of the art, having the teachings of Okayama and Stam before him at the time the invention was made, to modify memory disclosed by Okayama to use memory as taught by Stam wherein there is less available memory than is needed to store all data. One of ordinary skill in the art would be motivated to make use of the memory in view of the teachings of Stam, as doing so would give the added benefit of lowering the cost of image processing (as taught by Stam above).

Neither Masuda nor Stam teach a clock conversion unit comprising a first counter circuit for generating write addresses of the memory on the basis of the first clock so that the data corresponding to the predetermined period are written over plural times and a second counter circuit for generating read addresses of the memory on the basis of the second clock so that the data corresponding to the predetermined period are from the memory over plural times.

Okayama teaches a television screen converter comprising memory addressing circuitry comprising a memory (25), a write clock generator (22), a read clock generator (23), a write address counter (27), a read start address generator (29) and a read address counter (28). The write counter circuit (27) starts counting on receipt of a writing start reference signal (horizontal sync signal from sync separator 21) indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the one horizontal line of data can be written into the memory over plural times (column 3, lines 1-60). The read counter circuit (28) for start counting from a reading start reference signal (from read start address generator 29) indicating a reference timing of starting data reading from the memory, and generating read

addresses of the memory so that the one horizontal line of data which are written in the memory can be read over plural times (column 3, lines 1-60). Okayama has the additional benefit of automatically extracting and converting data from a wide screen version to a normal screen version (column 2, lines 11-17).

It would have been obvious to one of ordinary skill of the art, having the teachings of Masuda, Stam and Okayama before him at the time the invention was made, to modify memory controllers disclosed by Masuda to use memory addressing circuitry as taught by Okayama. One of ordinary skill in the art would be motivated to make use of the memory addressing circuitry in view of the teachings of Okayama, as doing so would give the added benefit of automatically extracting and converting data from a wide screen version to a normal screen version (as taught by Okayama above).

Neither Masuda, Stam nor Okayama teach the memory address setting method comprising: determining a broadcasting system of the digital video signal inputted to the first video processing unit, detecting upper limits or lower limits of count values of the first and second counter circuits corresponding to the determined broadcasting system, according to the broadcasting system or setting the detected upper limits or lower limits of the count values on the first and second counter circuits.

Worrell teaches a memory management process for video digital data that is capable of detecting/buffering various video format schemes via field type detector (78) found in video input interface (12); (column 1, lines 25-30 and column 5, lines 25-43). Also, Worrell teaches a method for addressing of video data unique to the format detected that addresses locations in memory (14) via memory controller (16) and video input interface (12); (column 3, lines 4-41).

In coordination with memory controller (16) and video input interface (12), counter limit values (L1 and L2) that writes/reads necessary data to/from memory (14). Worrell has the additional feature of providing a process to buffer various video data formats (column 1, lines 25-30).

It would have been obvious to one of ordinary skill of the art, having the teachings of Masuda, Stam, Okayama and Worrell before him at the time the invention was made, to modify memory address setting method taught by Masuda, Stam and Okayama to use a field type detector circuit as well as the counter limiting detectors as taught by Worrell. One of ordinary skill in the art would be motivated to make use of the addressing schemes in view of the teachings of Worrell, as doing so would give the added benefit of providing a process to buffer various video data formats (as taught by Worrell above).

Response to Arguments

Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or (571) 272-1000.

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September 22, 2006

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